SECTION 17

HIGH SPEED DACs AND DIRECT DIGITAL SYNTHESIS

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- DACs DESIGNED FOR MAXIMUM DYNAMIC RANGE
- WIDE DYNAMIC RANGE DDS SYSTEMS
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SECTION 17

HIGH SPEED DACs AND DIRECT DIGITAL SYNTHESIS

Walt Kester

High speed DACs have many applications in waveform reconstruction and direct digital synthesis (DDS). A new class of function generators called Arbitrary Waveform Generators (ARBs) allow a wide variety of complex waveforms to be programmed into a memory and then read out through a DAC.

Graphics display systems also utilize high speed DACs to direct and/or modulate the scanning electron beam across the CRT screen. A special type of DAC, sometimes referred to as a VIDEODAC, contains functions which allow ease of use in raster scan display systems. Some videodacs, called RAMDACs, contain on-chip color palette memories and provide even more functionality in graphics display systems.

HIGH SPEED DAC APPLICATIONS

- Instrumentation:
  - Waveform Reconstruction,
  - Arbitrary Waveform Generators
- Direct Digital Synthesis:
  - Receiver Local Oscillators
  - Frequency Hopping Radios
  - Communications Systems
  - QAM Systems
  - Radar Systems
- Graphics Display Systems:
  - Vector Scan
  - Raster Scan - Videodacs, Ramdacs

Figure 17.1

SETTLING TIME

Modern fast DACs generally have input registers which drive the internal switches as shown in Figure 17.2. The input latches minimize time-skew between the signals driving the switches and minimize signal-dependent glitches.

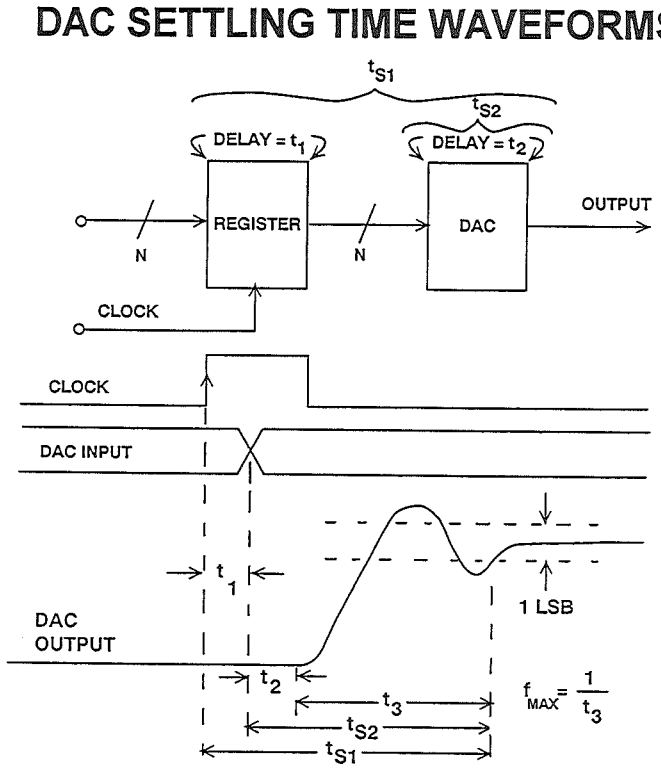


Figure 17.2

The settling time of a DAC is traditionally defined as the time from the digital input transition (usually measured from the 50% point) until the DAC output settles to within a certain error band (usually ±1/2 LSB) which is centered around the final value. As shown in Figure 17.2, a portion of the settling time may be due to a fixed propagation delay through the switches. If the DAC has a set of input latches or registers, the settling time should be measured from the 50% point of the latch strobe or register clock. Fullscale DAC settling time is measured for a digital input transition from 000...0 to 111...1. Midscale settling time is measured for a digital transition from 011...1 to 100...0 or 100...0 to 011...1.

It is often more useful to define DAC settling time with respect to the output alone as shown in Figure 17.3. Settling time is measured from the time the output leaves a ±1/2 LSB error band centered around the initial value until the time the output remains within a ± 1/2 LSB error band centered around the final value. The maximum DAC update rate allowable for ±1/2 LSB fullscale settling time then becomes $f_{max} = 1/t_S$. Faster update rates can be used if sample-to-sample changes in the DAC input are limited to values less than fullscale.

SETTLING TIME DEFINED WITH RESPECT TO DAC OUTPUT

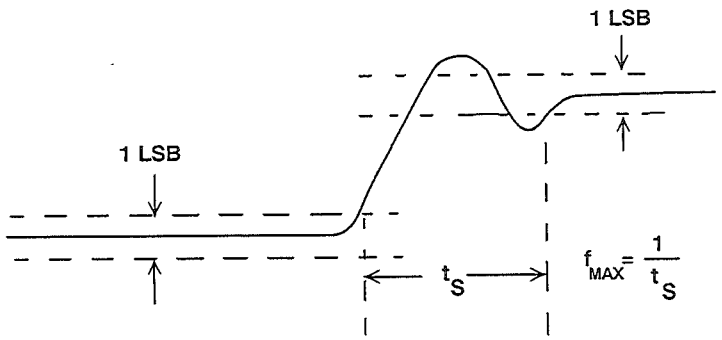


Figure 17.3

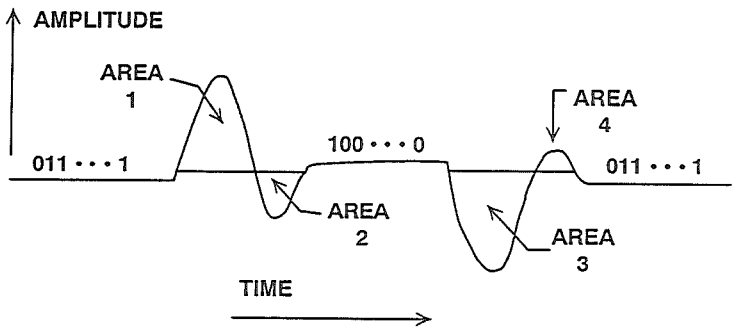
GLITCH IMPULSE AREA

Glitch impulse area is best understood by examining the waveform shown in Figure 17.4. The worst DAC glitches occur because of digital input logic skew and unequal propagation delays through the DAC switches (but there are other types, a noteworthy exception to this being the sigma-delta DAC architecture). These glitches are usually largest at the midscale transition because all bits in the DAC are changing at this point. The glitch produced by the 011...1 to 100...0 transition is usually different from that produced by the 100...0 to 011...1 transition, so each must be analyzed. Glitch impulse area is simply the area of a particular glitch, and is usually measured in the units of pV-sec, therefore the fullscale output voltage of the DAC must be known in order to make meaningful comparisons between DACs. The term *glitch energy* is incorrect since the unit pV-sec is *not* a measure of energy.

From Figure 17.4 it is clear that there are six possible glitch impulse areas to deal with. There are two glitch impulses associated with each transition. Their respective areas are designated 1,2,3, and 4. In addition, it is also useful to consider the *net glitch impulse* area associated with each of the two transitions. There are, respectively, AREA 1 – AREA 2, and AREA 3 – AREA 4. Examining the glitch impulse area specification on a DAC data sheet can lead to confusion unless a considerable amount of clarification is provided by the manufacturer.

Glitch impulse area remains constant regardless of filtering. Fast settling time does not always imply low glitch impulse. The desirable situation is for the DAC to have a net glitch impulse area of zero for each of the two transitions, i.e., AREA 1 – AREA 2 = AREA 3 – AREA 4 = 0. In the ideal case, of

GLITCH IMPULSE WAVEFORMS



GLITCH IMPULSE AREAS: AREA 1
AREA 2
AREA 3
AREA 4

NET GLITCH IMPULSE AREAS: | AREA 1 - AREA 2 |
| AREA 3 - AREA 4 |

Figure 17.4

AD9720 10-BIT, 400MSPS DAC MIDSCALE GLITCH IMPULSE WAVEFORM

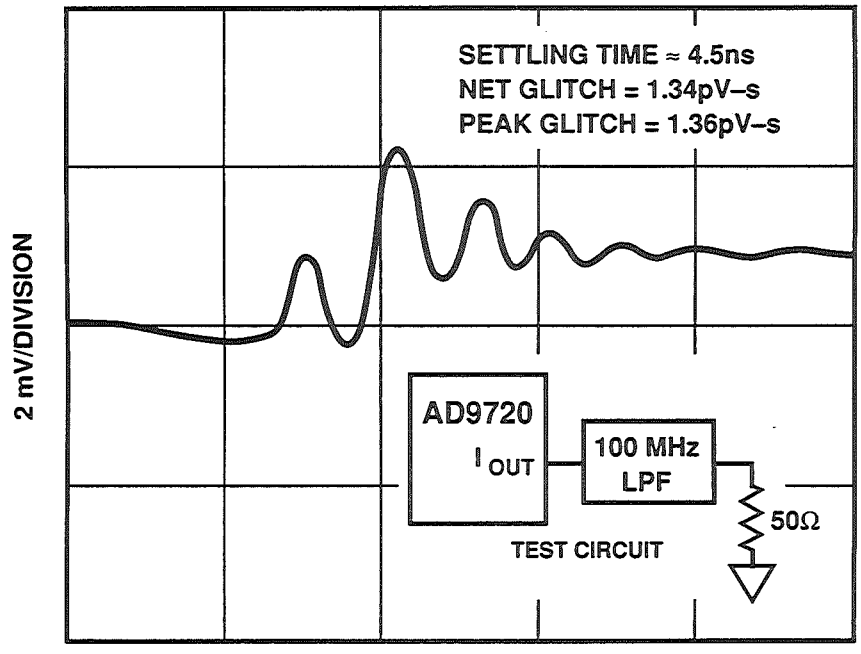


Figure 17.5

course, each of the four areas would be zero. A typical glitch impulse waveform for the AD9720 10-bit, 400MSPS DAC is shown in Figure 17.5. The waveform is for the midscale transition, and shows a net glitch area of 1.34pV-s, and a settling time of about 4.5ns.

HARMONIC DISTORTION AND SPURIOUS FREE DYNAMIC RANGE

Because the net glitch impulse area is code-dependent, it will produce both out-of-band and in-band harmonics when the DAC is reconstructing a sinewave. A net midscale glitch occurs twice during a single cycle of the reconstructed sinewave (at each zero crossing) and, therefore, will produce a second harmonic of the sinewave as shown in Figure 17.6. Note that higher order harmonics of the sinewave which alias back into the Nyquist bandwidth are not filterable. It is difficult to predict the harmonic distortion caused by a specified net glitch impulse area, therefore, both specifications are required to adequately evaluate the dynamic performance of a reconstruction DAC.

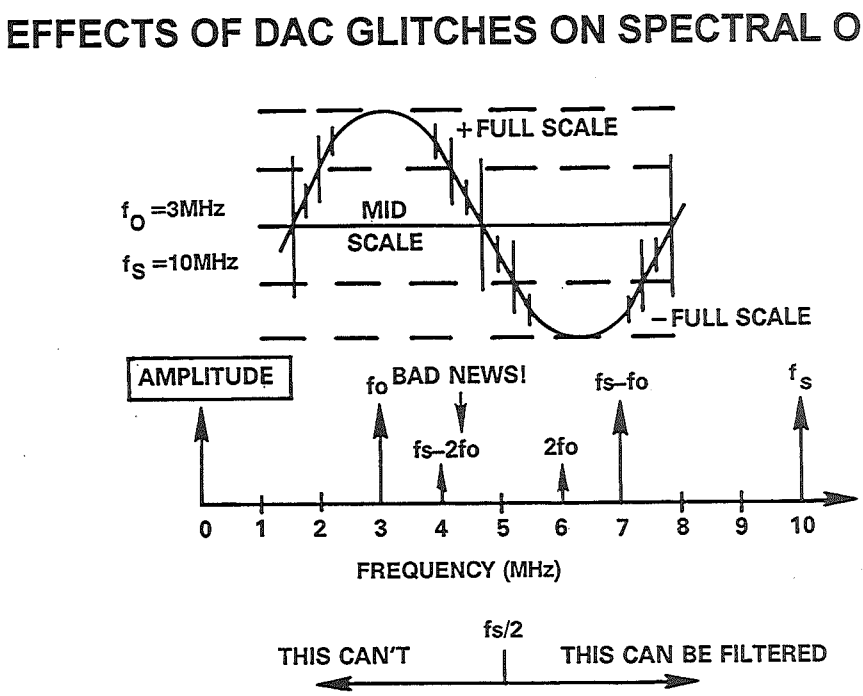


Figure 17.6

DACs Designed For Maximum Dynamic Range

Two fundamental high speed DAC architectures are shown in Figure 17.7. The first method switches equally-weighted currents into an R-2R resistor ladder network which performs the binary weighting. In the second method, the currents are binarily weighted and are switched into a load resistor. Many high speed DACs often use a combination of the above methods.

The large signal-dependent glitches produced by straight binary DACs generate unwanted harmonics of digital input signal. Many high speed DACs use a combination of several techniques to achieve small glitch and wide dynamic range.

If real estate, cost, power, and capacitance were of no consideration, the ideal "glitchless" DAC would consist of $2^N - 1$ equally weighted current switches preceded by latches and decoding logic as shown in Figure 17.8. The glitch produced by switching between levels is code-independent and, therefore, does not generate harmonics of the sinewave being reconstructed. It produces energy at the update rate (and also at multiples of the update rate) which can be filtered from the DAC output. The residual energy causes only a constant dc offset in the output signal. A set of latches is required after the binary decoding logic in order to equalize the delays to the actual switches themselves. The switches are designed using low-level logic levels to minimize coupling to the output.

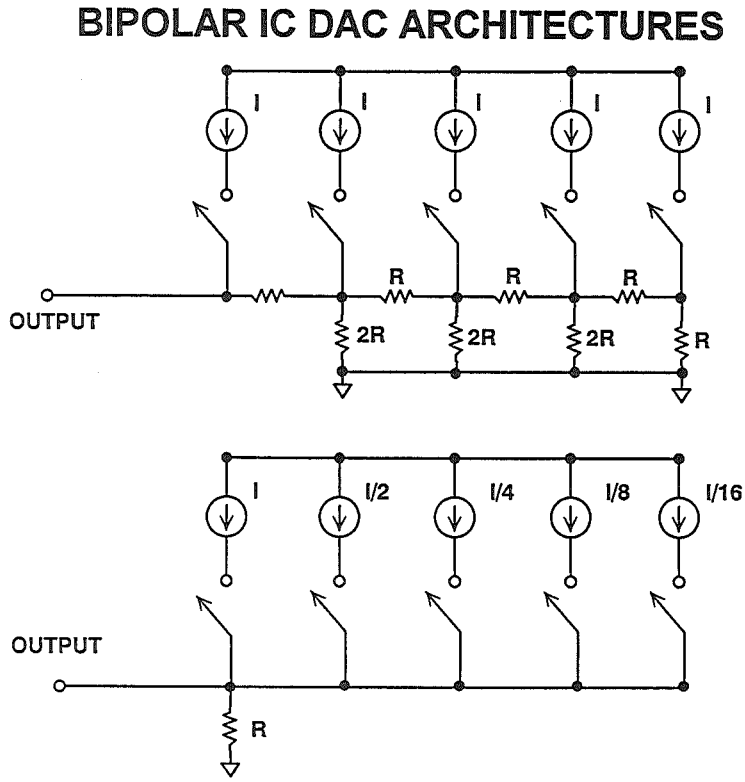


Figure 17.7

IDEAL DAC ARCHITECTURE FOR MINIMUM CODE-DEPENDENT GLITCH

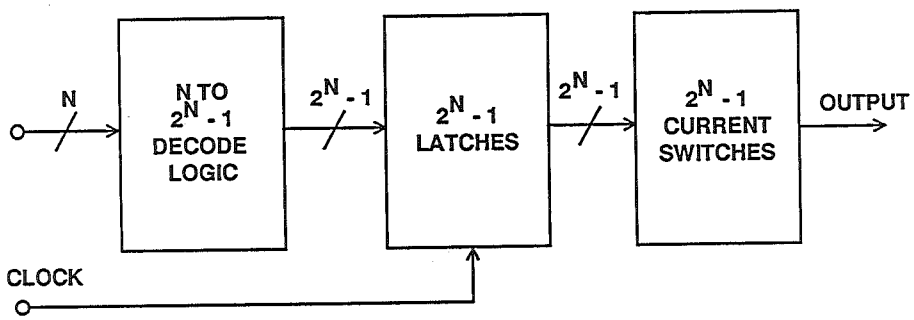


Figure 17.8

Obviously, this scheme is not practical for high resolution DACs, but is often used for the 4 to 6-bit DACs which are used as building blocks in subranging ADCs.

A significant amount of glitch reduction can be achieved by applying the above concept to the first few MSBs of a high resolution DAC in a technique called *segmentation*. This technique is often used in audio DACs.

A block diagram of the AD9712B 12-bit 100MSPS DAC is shown in Figure 17.9 to illustrate the segmented architecture. The four MSBs are decoded into a thermometer code which drives 15 equally weighted current switches after latching. The remaining bits are obtained using binary current weighting (bits 5 and 6) and R-2R current division (bits 7-12). Segmentation of the four MSBs reduces the effects of the midscale glitch impulse by a factor of 16 compared to the glitch which would result if straight binary decoding were employed. This technique used in the AD9712B achieves a glitch area of less than 28pV-s as shown in Figure 17.10.

SEGMENTED ARCHITECTURE USED IN THE AD9712B (ECL) AND AD9713B (TTL) DACs

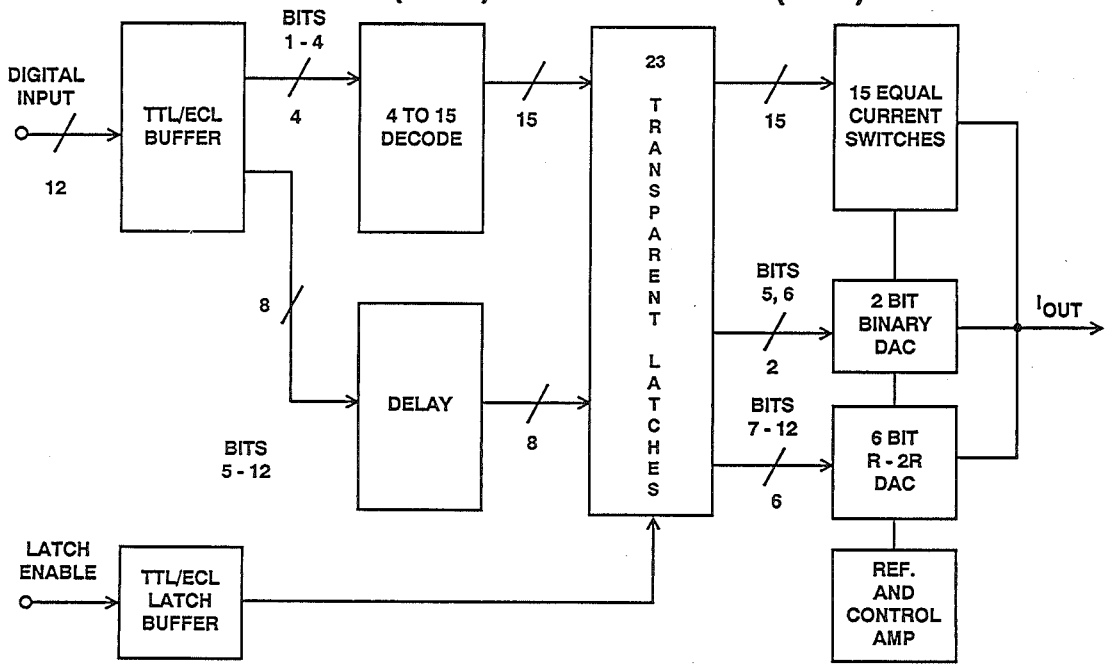


Figure 17.9

AD9712B/AD9713B MIDSCALE GLITCH IMPULSE AND FULLSCALE OUTPUT SIGNAL

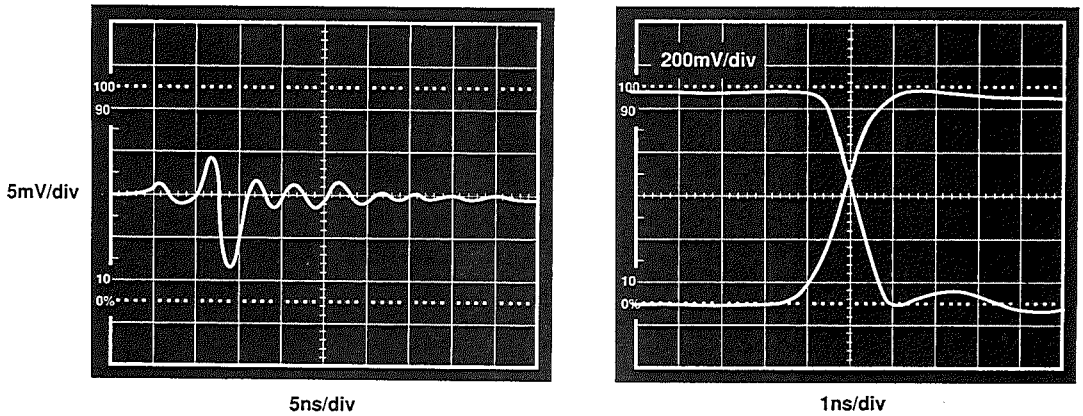


Figure 17.10

WIDE DYNAMIC RANGE DDS SYSTEMS

A simple circuit for generating a digital sinewave using a PROM and a DAC is shown in Figure 17.11. Each location in the PROM corresponds to a discrete sample of the sinewave. The PROM must contain an integral number of cycles in order to prevent a discontinuity when the PROM rolls over. This approach is limited, however, because the sinewave frequency can only be changed by varying the clock rate or by reprogramming the PROM.

A much more flexible scheme is shown in Figure 17.12 and is the basis of modern DDS techniques. The circuit driving the DAC is often referred to as a Numerically Controlled Oscillator (NCO) and serves the same function as the PROM in the simple DDS system described above.

SIMPLE DDS SYSTEM

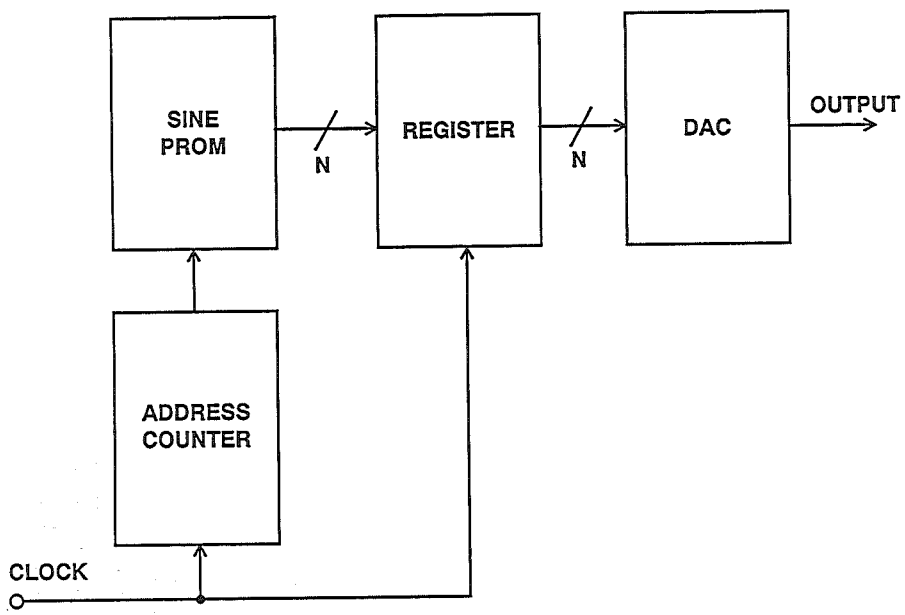


Figure 17.11

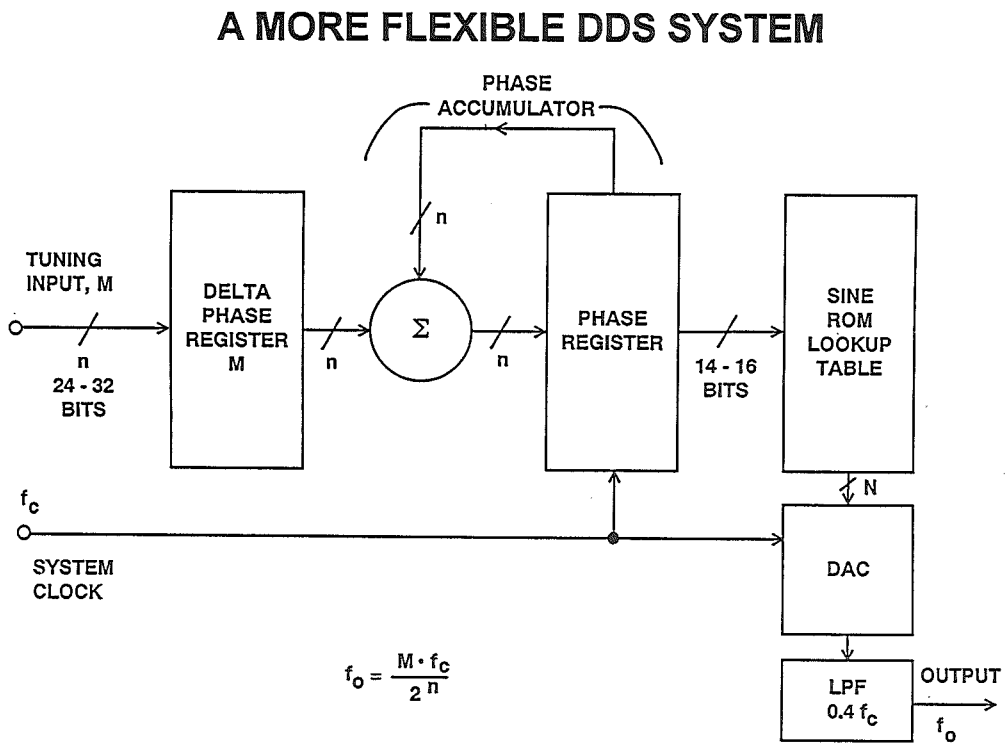
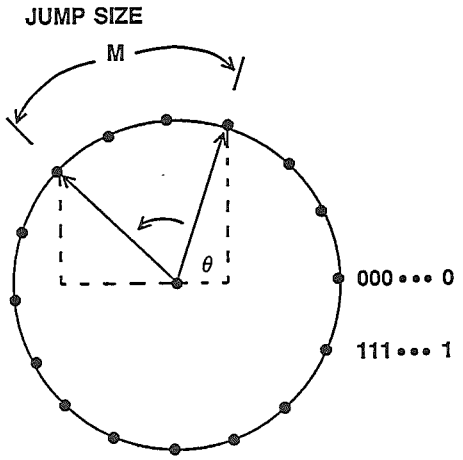


Figure 17.12

In order to understand the system, first consider a sinewave oscillation as a vector rotating around a phase circle as shown in Figure 17.13. Each point on the phase circle corresponds to a particular point on the output waveform. As the vector travels around the phase circle, the corresponding output waveform is generated. One revolution on the phase circle corresponds to one cycle of the sinewave. A phase accumulator is used to perform the linear motion around the phase circle. The number of discrete points on the phase circle is determined by the resolution of the phase accumulator. For an n-bit accumulator, there are 2^n points on the phase circle. The digital word in the delta phase register (M) represents the "jump size" between updates. It commands the phase accumulator to increase by M points on the phase circle each time the system is clocked. If M is the number stored in the delta phase register, f_c is the clock frequency, and n is the phase accumulator resolution, then the frequency of rotation around the phase circle (the output frequency) is given by $f_o = M \cdot f_c / 2^n$, which is known as the "tuning equation."

PHASE ACCUMULATOR OSCILLATOR



DIGITAL PHASE CIRCLE

$$f_o = \frac{M \cdot f_c}{2^n}$$

n	NUMBER OF POINTS
8	256
12	4096
16	65536
20	1048576
24	16777216
28	268435456
32	4294967296

Figure 17.13

The frequency resolution of the system is $f_c / 2^n$ which represents the smallest incremental frequency capable of being produced. The delta-phase register and the accumulator are typically 24 to 32 bits wide.

The output of the phase accumulator drives the address input of a sinewave ROM lookup table in which is stored amplitude information for exactly one cycle of a sinewave. The ROM drives a DAC which reconstructs the analog sinewave. The phase data is usually truncated in order to minimize the size of the ROM and the resolution of the DAC. The phase resolution (corresponding to the number of locations in the ROM) directly affects the spectral purity of the output. For example, if the phase information is truncated to 15 bits, the theoretically largest phase spur is about 90dB below fullscale (neglecting DAC spurs).

A functional block diagram of the AD9955 85MHz Direct Digital Synthesizer is shown in Figure 17.14. It comprises a 32-bit phase accumulator and a 15-bit phase-to-12-bit sine amplitude converter. The phase to sine amplitude converter calculates the sine amplitude using a proprietary algorithm for the first 90° of the sine cycle, and takes advantage of the symmetry of the waveform to calculate the remaining quadrants. Truncation of the phase information to 15-bits and the output data to 12-bits results in a 90dB SFDR as shown in the calculated response of Figure 17.15. The control logic is CMOS compatible, and the clock input is TTL. CMOS outputs are latched on board, and a data ready signal is provided.

AD9955 85MHz DIRECT DIGITAL SYNTHESIZER

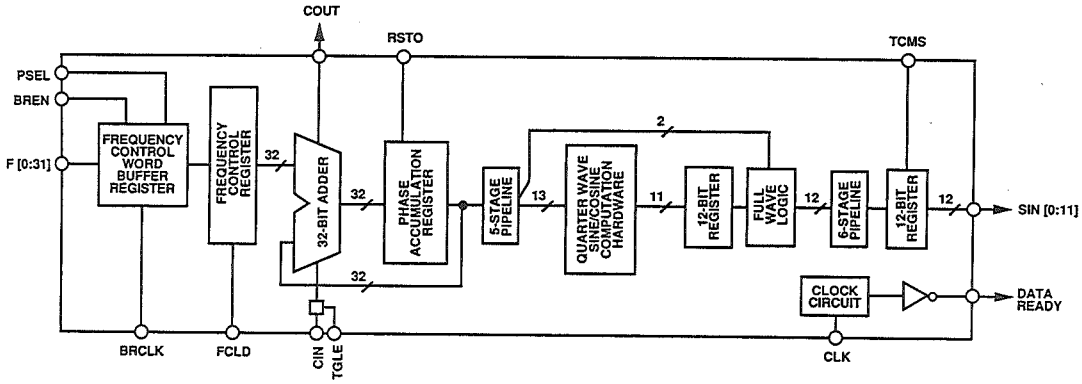


Figure 17.14

AD9955 OUTPUT SPECTRUM (CALCULATED) SHOWS 90dB SFDR FOR 15-BIT PHASE TRUNCATION AND 12-BIT OUTPUT DATA TRUNCATION

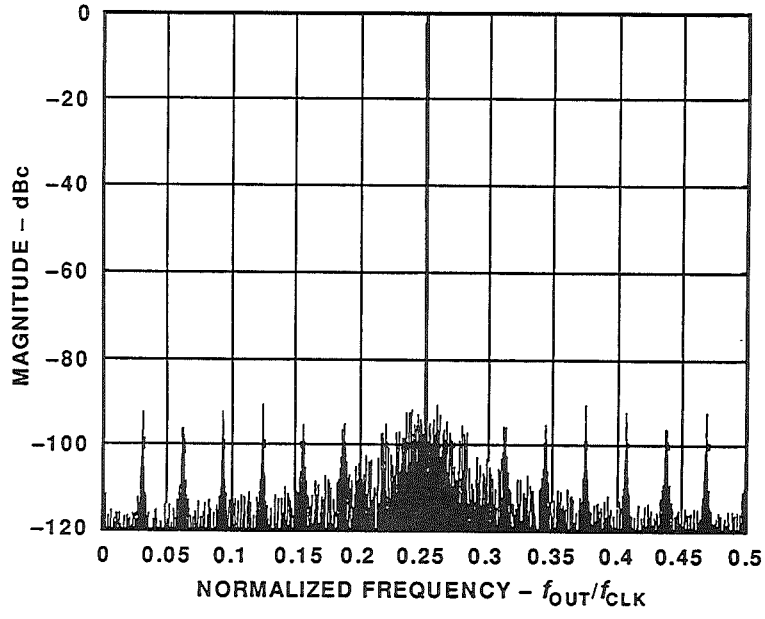


Figure 17.15

Exceptional SFDR performance can be obtained using the AD9955 DDS with the AD9721 10-bit, 100MSPS low glitch DAC as shown in Figure 17.16. As in all high speed applications, proper layout is critical. Analog signal paths should be kept as short as possible and properly terminated to avoid reflections. Digital signal paths should be kept short and run lengths matched to avoid propagation delay mismatch. The digital runs must be kept away from the analog runs and the clock run. The 130Ω series resistors are inserted between the AD9955 outputs and the AD9721 inputs to reduce data feedthrough effects which could impair spectral purity. Layout of the ground circuit is critical. A single, low impedance ground plane is essential. Power supplies should be decoupled to the ground with low inductance ceramic chip capacitors.

An evaluation board (see Figure 17.17) is available which combines the AD9955 and either the AD9713B, an 80MSPS 12-bit DAC, or the AD9721, a 10-bit 100MSPS DAC, both of which are supplied with the board.

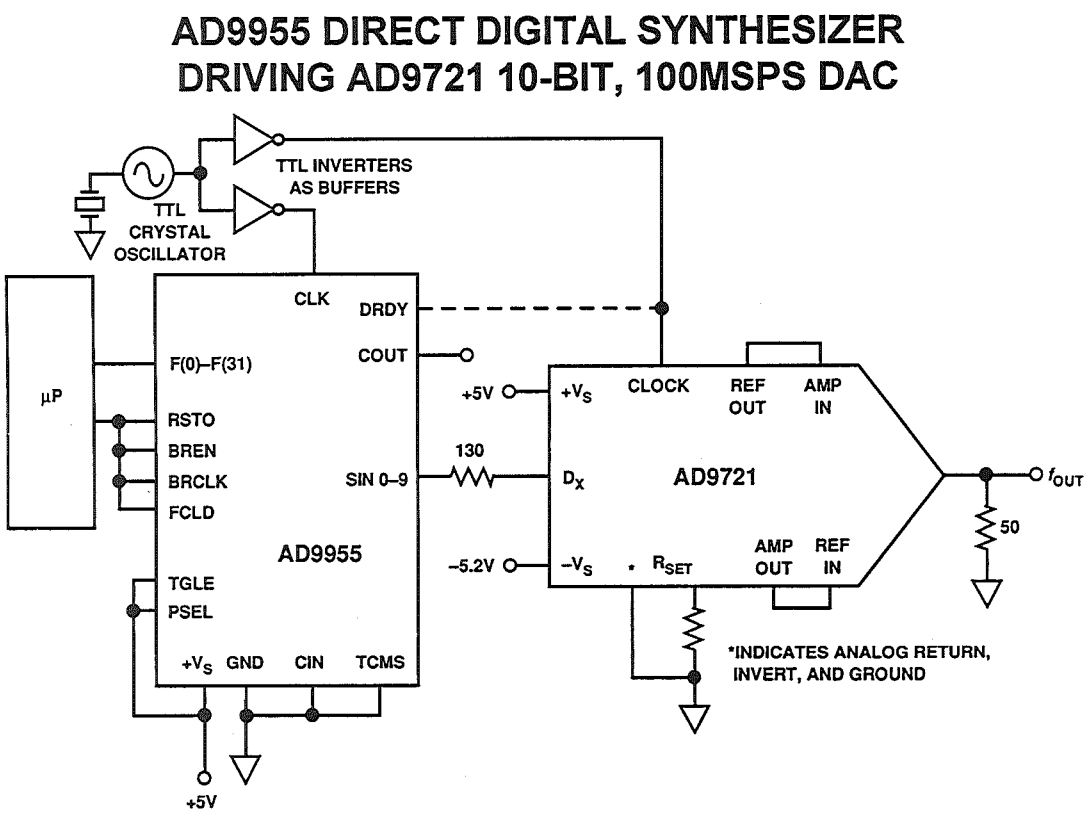


Figure 17.16

AD9955 DDS EVALUATION BOARD SETUP

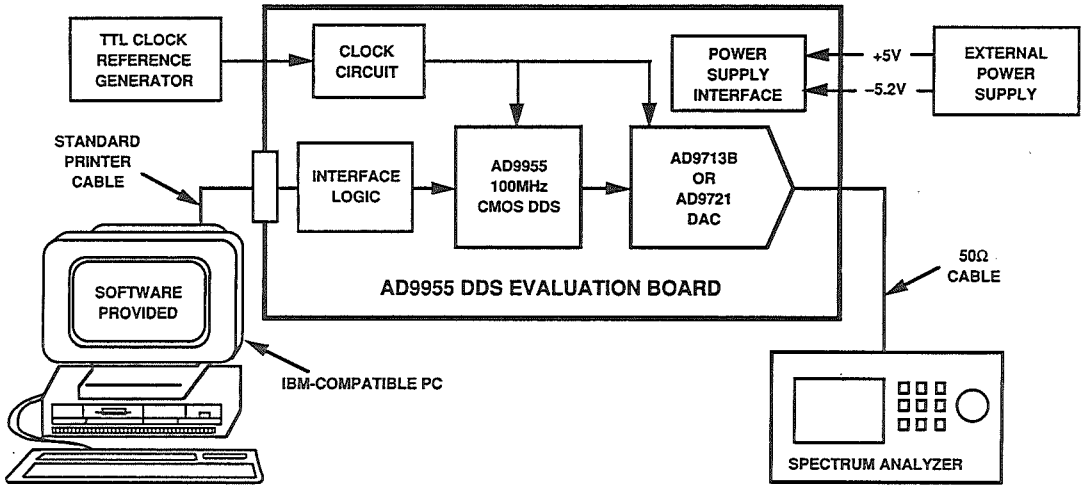


Figure 17.17

AD9720 (400MSPS, ECL) / AD9721 (100MSPS, TTL) LOW-GLITCH, HIGH SFDR RECONSTRUCTION DACS

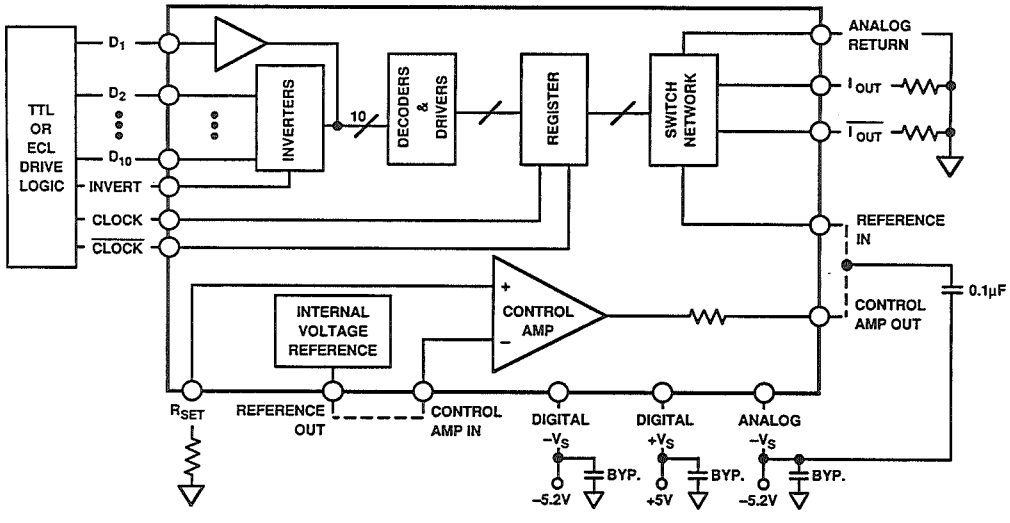


Figure 17.18

AD9720/AD9721 DAC MIDSCALE GLITCH SHOWS 1.34pV-s NET IMPULSE AREA AND SETTLING TIME OF 4.5ns

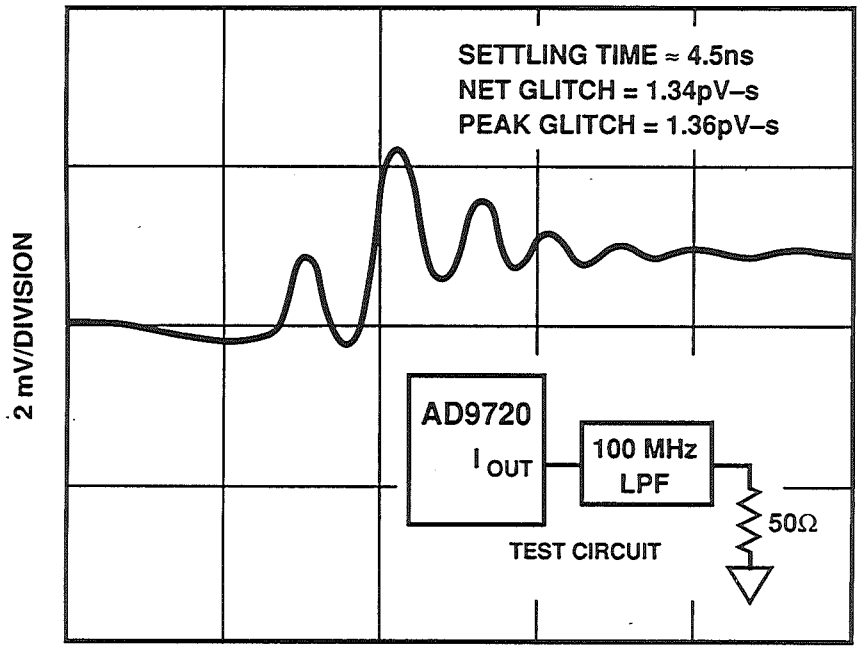
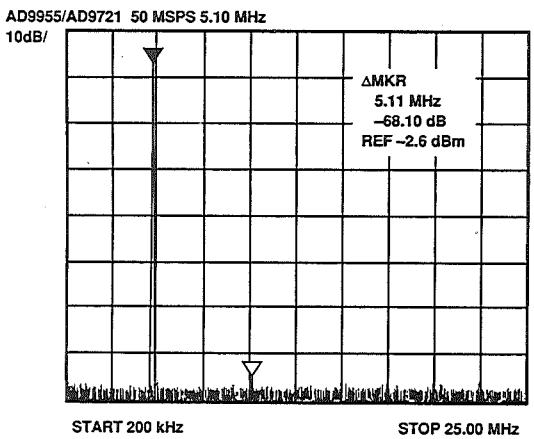


Figure 17.19

AD9955 DDS AND AD9721 DAC PERFORMANCE AT 50MSPS

OUTPUT = 5.10MHz



OUTPUT = 16.60MHz

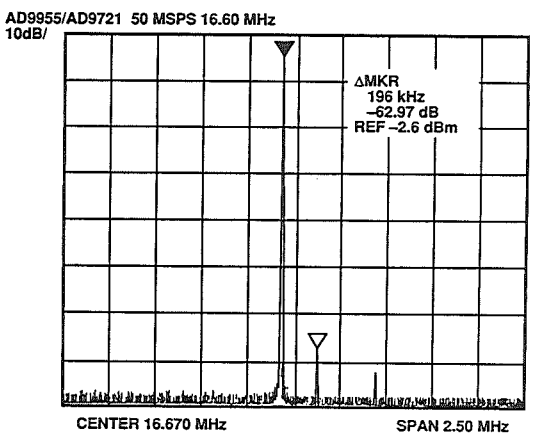


Figure 17.20

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The AD9720 (400MSPS ECL) / AD9721 (100MSPS TTL) 10-bit DACs are designed specifically for low glitch and high SFDR in DDS applications. A block diagram of the DAC is shown in Figure 17.18, and the glitch impulse waveform in Figure 17.19.

Typical 50MSPS performance of the AD9955 driving the AD9721 on the evaluation board is shown in Figure 17.20, and 100MSPS performance is Figure 17.21. Note that a SFDR of between 63 and 68dB is obtained in all cases.

High speed CMOS technology allows the complete integration of the DDS oscillator and the DAC on a single chip.

The AD7008 DDS Modulator integrates a 32-bit phase accumulator with a 10-bit DAC on the same chip. A block diagram of the device is shown in Figure 17.22. The maximum clock rate for the device is 50MSPS yielding usable analog outputs to about 20MHz. An on-chip amplitude modulator contains two multipliers fed with sine and cosine values from a ROM lookup table, and with amplitude values loaded from either the parallel or serial port. When loaded with quadrature data, the sum of the two multipliers provides a single-sideband RF signal output. A power-down pin allows external control of a power-down mode (also accessible through the microprocessor interface.

AD9955 DDS AND AD9721 DAC PERFORMANCE AT 100MSPS

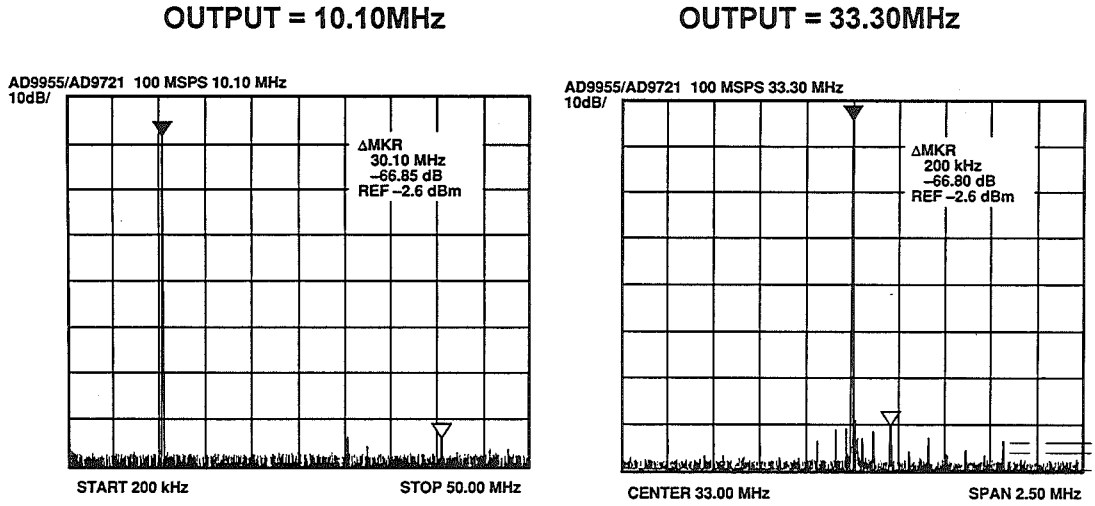

Figure 17.21

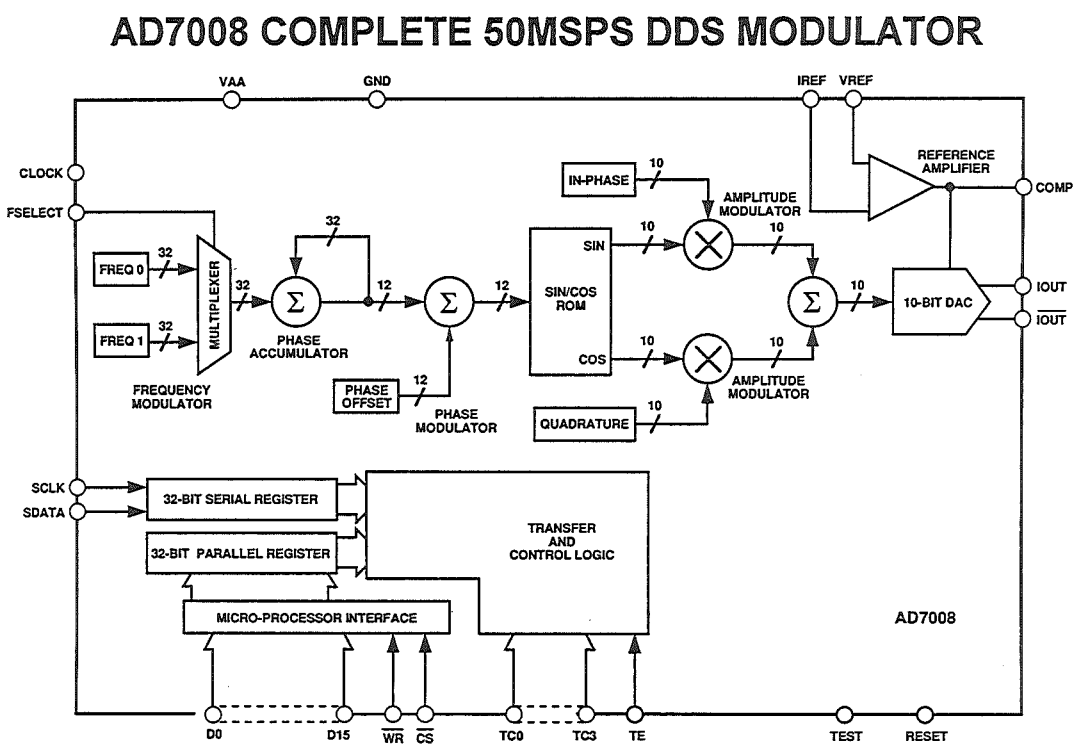

Figure 17.22

INJECTING DIGITAL DITHER IN DDS SYSTEMS TO INCREASE SFDR

Since a DDS system is a sampled data system, the DAC output sinewave has quantization noise superimposed on the fundamental sinewave output. Although the rms value of this noise in the bandwidth dc to $f_S/2$ is $q/\sqrt{12}$, certain ratios between the clock frequency and the output frequency may cause this noise to concentrate in harmonics of the fundamental sinewave, thereby degrading the SFDR. In the case of ADCs, a small amount of broadband noise (rms value of 1/2 LSB) is added to the ADC input to randomize the quantization noise spectrum. The same thing can be done in a DDS system as shown in Figure 17.23 (see Reference 1). The pseudo-random digital noise generator output is added to the DDS sine amplitude word before being loaded into the DAC. The amplitude of the digital noise is set to about 1/2 LSB. This accomplishes the randomization process at the expense of a slight increase in the overall output noise floor.

INJECTION OF DIGITAL DITHER IN A DDS SYSTEM TO RANDOMIZE QUANTIZATION NOISE AND INCREASE SFDR

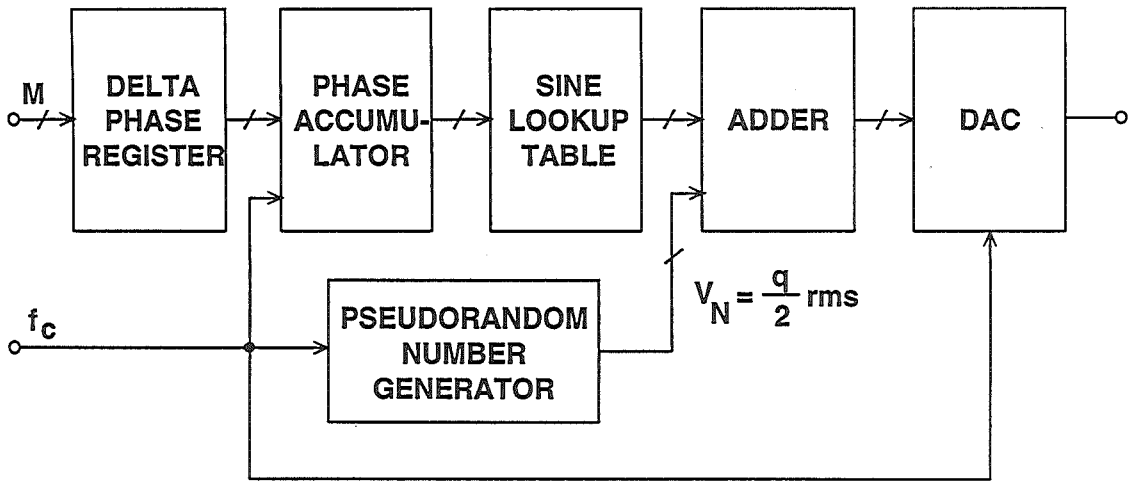

Figure 17.23

DEGLITCHING DACS USING SHAS

SHAs such as the AD9100 and AD9101 can be used to deglitch DACs as shown in Figure 17.24. Just prior to latching new data into the DAC, the SHA is put into the hold mode so that the DAC switching glitches are isolated from the output. The switching transients produced by the SHA are code-independent and occur at the update frequency and hence are easily filterable. However, when using a high performance low glitch DAC such as the AD9712B/ AD9713B or the AD9720/AD9721 there may only be marginal improvement.

SIN(X)/X FREQUENCY ROLLOFF EFFECT

The output of a reconstruction DAC can be visualized as a series of rectangular pulses whose width is equal to the reciprocal of the update rate as shown in Figure 17.25. Note that the reconstructed signal is down 3.92dB at the Nyquist limit with respect to the low frequency value. An inverse sin(x)/x filter is sometimes placed after the DAC to correct for this effect.

DEGLITCHING A DAC OUTPUT USING A SAMPLE-AND-HOLD

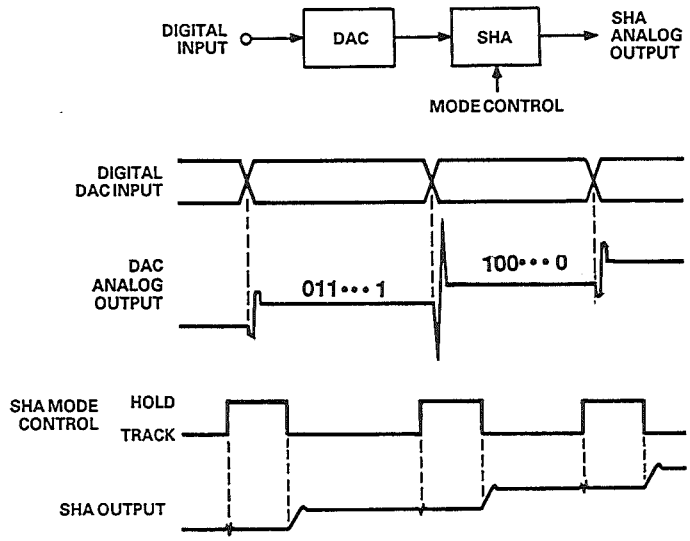

Figure 17.24

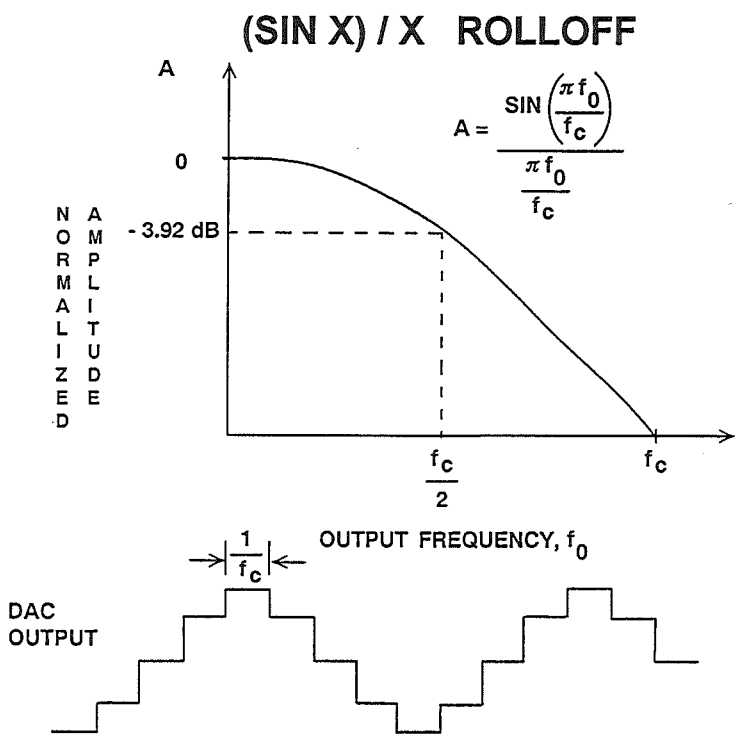

Figure 17.25

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2. Henry T. Nicholas, III and Henry Samueli, *An Analysis of the Output Spectrum of Direct Digital Frequency Synthesizers in the Presence of Phase-Accumulator Truncation*, **IEEE 41st Annual Frequency Control Symposium Digest of Papers**, 1987, pp. 495-502, IEEE Publication No. CH2427-3/87/0000-495.

3. Henry T. Nicholas, III and Henry Samueli, *The Optimization of Direct Digital Frequency Synthesizer Performance in the Presence of Finite Word Length Effects*, **IEEE 42nd Annual Frequency Control Symposium Digest of Papers**, 1988, pp. 357-363, IEEE Publication No. CH2588-2/88/0000-357.